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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/587,052	06/02/2000	Timothy John Lindquist	169.17	6630

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/587,052	LINDQUIST, TIMOTHY JOHN	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17 and 18* is/are allowed.

6)☒ Claim(s) *1-8,11,12,15 and 16* is/are rejected.

7)☒ Claim(s) *9,10,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/23/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-18 are presented for examination.

2. Claims 1-8,11,12,15,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennings , III et al. (5,357,152) in view of Chamdani et al. (6,112,019) in view of Oliver et al. (5,491,694).

3. As to claim 1, Jennings disclosed a parallel reconfigurable (e.g. programmable) system comprising at least :

a) a plurality of processing units (e.g. see fig.2);

b) communication means [programmable circuit] by which the plurality of processing units were interconnected (e.g. see the programmable circuit and its configurable signal bus LSF and LSC in fig.2); wherein the communication medium was dynamically configurable based on program (e.g. programmable) to be processed such that the processing units can selectively arranged in at least a first and second distinct configurations (see integer and the floating point selections in col.7, lines 36-40, see also col.5, lines 1-27).

4. Jennings did not specifically show his the second configuration [floating point] had deeper pipeline depth than the first configuration [integer] as claimed. However, Chamdani disclosed a system including a second configuration [floating point] which had a deeper pipeline stage than a first configuration [integer (e.g. see fig.13, col.32, lines 19-38). It would have been obvious to one of ordinary skill in the art to use Chamdani in Jennings for including the deeper pipeline configuration as claimed.

because the use of Chamdani could enhance the processing ability of Jennings to increase the precision level of the operation results, and thereby maximizing the throughput of the functional elements in the system, and it could be readily done by defining the deeper pipeline configuration of Chamdani into the configuration file of Jennings such that the greater number of the pipeline stages of Chamdani could be recognized by Jennings, therefore increasing the processing power of Jennings, and in doing so, provided a motivation.

5. Jennings did not specifically teach the common bus for the packetized data as claimed. However, Oliver disclosed a system including a common bus used as a packet data bus (see Col.11, lines 11-19). It would have been obvious to one of ordinary skill in the art to use Oliver in Jennings for including the packet data common bus as claimed because the use of Oliver could provide the control ability of Jennings to accept data in a single integrated bus format, thereby minimizing the hardware overheads of the system, and it could be readily achieved by configuring the common bus into Jennings with modified interface parameter, such as the bus width, and W/R ports, so that the common bus of Oliver could be recognized by Jennings in order to provide the enhanced bus structure , and for the above reasons, provided a motivation.

6. As to the dynamic configurable feature, Jennings disclosed that his invention contemplates the use of one or more logic networks that can perform a variety of logic functions either by configuration of a multi-function network or by sub-networks each perform one or more dedicated functions (col.1, lines 41-47), and this can permit smaller size programmable logic gate or memory array to be used to control a logic

operation of a given complexity, or a given size of array to control more complex operations (col.1, lines 65-68). Therefore, Jennings is very flexible (see also selected desired logic function performed by the logic network in col.2, lines 66-68, see the corresponding enabling signals for ALUS in different clusters in col.6, lines 29-35). Moreover, Jennings logic network can be integrated with groups of memory cells which can be selectively activated (e.g. see col.2, lines 7-18), therefore, the configuration of Jennings network was dynamic.

7. Jennings is used as primary reference because it shows clearly the structure of the plurality of processing units. Chamdani is used to supplement the teaching of the deeper pipeline. Oliver is used for providing the teaching of the packet common bus connection.

8. As to claim 2, Jennings also included logic configurations (see the signal changes in col.4, lines 50-68).

9. As to claim 3, Jennings also included data bus (e.g. see col.4, lines 5-8, see also the data bus DA at a given cycle time).

10. As to claim 4, Jennings also included the control means for transmission and reception of the data (see the data transfer from the source to destination in col.3, lines 62-68, col.4, lines 1-8).

11. As to claim 5, Jennings did not specifically show the packet data bus as claimed. However, Jennings was directed to a network configuration (e.g. see col.1, lines 41-52).

Therefore, packet data bus was most likely in Jennings since the transfer of packet data format had been a characteristic feature of the network communications.

12. As to claim 6, Chamdani also included VLIW (e.g. see col.36, lines 9-35).

13. As to claim 7, Jennings taught a programmable circuit which must have a program compiler to compile the program, otherwise , it would not have functioned properly.

14. As to claim 8, Jennings did not explicitly show the image data as claimed. However, Jennings, in the same patent, disclosed a SIMD (col.3, lines 36-41) which was a characteristic processing feature of a image processing, therefore, the image data was also applicable in Jennings.

15. As to claims 11,12, Jennings did not specifically show the arrangement of different number of processing units in pipeline layers as claimed. However, Chamdani disclosed different processing units (integer and floating point units) had arranged in different pipeline layers (see the seven and ten stage deep in col.32, lines 21-32). It would have been obvious to one of ordinary skill in the art to use Chamdani in Jennings for including the different pipeline layers as claimed because the use of Chamdani could increase the control capability of Jennings to achieve a predetermined set of precision level of the operation results, and thereby optimizing the throughput of the functional elements in the system, and it could be readily done by defining the deeper pipeline configuration of Chamdani into the configuration file of Jennings such that the different number of the pipeline stages of Chamdani could be recognized by Jennings,

therefore increasing the processing power of Jennings, and in doing so, provided a motivation.

16. Jennings did not specifically teach the common bus for the packetized data as claimed. However, Oliver disclosed a system including a common bus used as a packet data bus (see Col.11, lines 11-19). It would have been obvious to one of ordinary skill in the art to use Oliver in Jennings for including he packet data common bus as claimed because the use of Oliver could provide the control ability of Jennings to accept data in a single integrated bus format, thereby minimizing the hardware overheads of the system, and it could be readily achieved by configuring the common bus into Jennings with modified interface parameter, such as the bus width, and W/R ports, so that the common bus of Oliver could be recognized by Jennings in order to provide the enhanced bus structure , and for the above reasons, provided a motivation.

17. As to the dynamic configurable feature, see discussions in paragraph 6 above.

18. As to claims 15,16, Jennings also directed to SIMD processing (e.g. see col.3, lines 35-43).

19. Claims 9,10, 13 ,14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the specific feed forward limitations of the image data with the first configuration and second configuration.

20. Claims 17 and 18 are allowable over the art of record for reciting the combined features of eh dynamically configurable communication means selectively arranged the processing un its in the first and second distinct configurations, the first configuration having a larger number of processing unit in parallel than the second configuration, the second configuration of deeper pipeline than that first configuration, the image data , the first configuration used for first type image processes having no necessity for feed forward of data calculation whilst the second configuration used for second type image having necessity for the feed forward data calculations .

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Cotton et al. (5,237,571) is cited for the background teaching of the reconfigurable data bus (see the associated switch ports in col.4, lines 42-68, col.5, lines 1-60).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162.

The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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